P24C512X

I²C-Compatible Serial E²PROM

Datasheet Rev.1.3

General Description

The P24C512X is I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 512 Kbits (64 Kbytes), which is organized in 128 bytes per page.

Features

- Single Supply Voltage and High Speed Mode
  - ✧ Minimum operating voltage down to 1.65V
  - ✧ 1 MHz clock from 1.65 V to 3.6 V
  - ✧ 3.4MHz clock from 1.65 V to 3.6 V
- Low power CMOS technology
  - ✧ Read current 0.15mA (400kHz, typical)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- 128 bytes Page Write Modes, Partial Page Writes Allowed
- Software Write Protection (SWP) for Programmable Block
  - ✧ Upper quarter, upper half, upper3/4, whole memory array
- Software Programmable Device ID Configuration
  - ✧ 2 BIT DSC Register and configured by DSCWR command
- Additional Write Lockable Page
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - ✧ Endurance: 1 Million Write Cycles
  - ✧ Data Retention: 100 Years
  - ✧ HBM: 4 kV
  - ✧ Latch up Capability: +/- 200mA(25C)
- Package:
  - ✧ WLCSP4 (Ball Pitch 400umx500um)
  - ✧ WLCSP4 (Ball Pitch 400umx400um)

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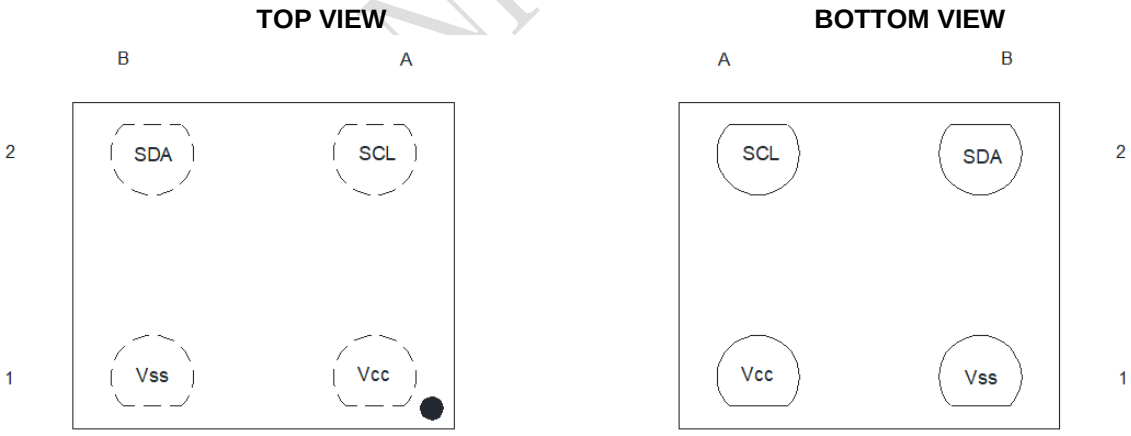
1. Pin Configuration

1.1 Pin Configuration

Figure 1-1 Pin Configuration

WLCSP4 (Ball pitch 400um*500um)



WLCSP4 (Ball pitch 400um*400um)

1.2 Pin Definition

Table 1-1Pin Definition for Package WLCSP4 (Ball Pitch 400um*500um)

Pin	Name	Type	Description
A1	Vcc	Power	Power Supply
A2	SCL	Input	Serial Clock Input
B1	SDA	I/O	Serial Data Input and Serial Data Output
B2	Vss	Ground	Ground

Table 1-2 Pin Definition for Package WLCSP4 (Ball Pitch 400um*400um)

Pin	Name	Type	Description
A1	Vcc	Power	Power Supply
A2	SCL	Input	Serial Clock Input
B1	Vss	Ground	Ground
B2	SDA	I/O	Serial Data Input and Serial Data Output

1.3 Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-OR'ed with any number of other open-drain or open-collector devices.

Supply Voltage (V_{CC}): V_{CC} is the supply voltage.

Ground (Vss): Vss is the reference for the V_{CC} supply voltage.

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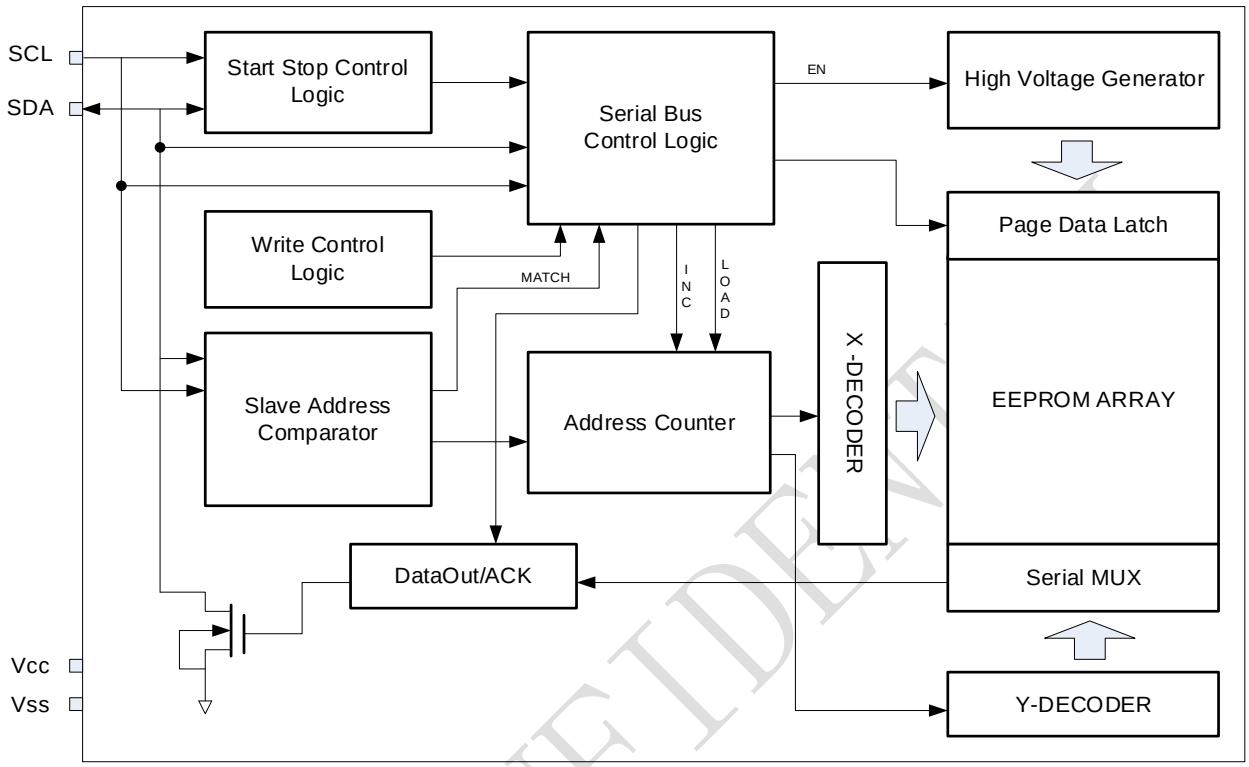
2. Block Diagram

Figure 2-1 Block Diagram



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3. Electrical Characteristics

Table 3-1 Absolute Maximum Ratings [1]

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient operating temperature	-40	85	°C
V_{CC}	Supply Voltage	-0.5	4.0	V
V_{IO}	Input or output range	-0.5	4.0	V
I_{OL}	DC output current (SDA=0)	-	5	mA

Note: [1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3-2 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input/output Capacitance (SDA)	8	pF	$V_{I/O}$=Vss
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN}=Vss

Note: [1] Test Conditions: T_A= 25°C, f_{SCL} = 1MHz, Vcc =3.3V.

Table 3-3 DC Characteristics （Unless otherwise specified, V_{CC} = 1.65 V to 3.6V, T_A= -40°C to+85°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.65	-	3.6	V	T_A = -40 °C to 85 °C
Isb	Standby Current (Standby mode)	-	0.1	3.0	uA	V_{CC} = 1.8V, Vin = V_{SS} or V_{CC} Device is not selected
I_{CC1}	Supply Current (Read)	-	0.15	0.5	mA	V_{CC} = 1.8 V, f_{SCL} = 400 kHz
		-	-	0.5	mA	V_{CC} = 3.6 V, f_{SCL} = 400 kHz
		-	-	1.0	mA	V_{CC} = 3.6 V, f_{SCL} = 1 MHz
		-	-	3.0	mA	V_{CC} = 3.6 V, f_{SCL} = 3.4 MHz
I_{CC2}	Supply Current (Write)	-	1.0	2.0	mA	During t_W, 1.65V < V_{CC}< 3.6 V
I_{LI}	Input Leakage Current	-2.0	-	+2.0	μA	V_{IN} = V_{CC} or Vss, device in standby mode
I_{LO}	Output Leakage Current	-2.0	-	+2.0	μA	SDA in Hi-Z, external voltage applied on SDA: Vss or Vcc
V_{IL}	Input Low Voltage	-0.45	-	0.3 V_{CC}	V	SCL, SDA
V_{IH}	Input High Voltage	0.7V_{CC}	-	V_{CC}+0.5	V	SCL, SDA
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 2.1 mA, V_{CC} = 2.5 V

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Table 3-4 Fast Mode AC Characteristics（T_A = -40 °C to +85 °C）

Symbol	Parameter	1.65≤V_{CC}≤3.6			1.65≤V_{CC}≤3.6			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.55	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.3	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.50	μs
t_I	Noise Suppression Time	-	-	0.05	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data in Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data in Setup Time	0.1	-	-	0.08	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.3	μs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- t_{AA} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 VCC or 0.7 VCC, assuming that Rbus × Cbus time constant is within 400 ns for 0.4 MHz frequency, within 120 ns for 1 MHz frequency
- RL (connect to VCC): 1.3 kΩ
- CL = 100 pF
- Input pulse voltage: 0.2 VCC to 0.8 VCC
- Input rise and fall time: < 50 ns
- Input and output timing reference voltage: 0.3 VCC and 0.7 VCC

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Table 3-5 High Speed Mode AC Characteristics （T_A= -40 °C to +85 °C）

Symbol	Parameter	1.65≤V_{CC}≤3.6			Units
		Min.	Typ.	Max.	
f_{SCL}	Clock Frequency	-	-	3400	kHz
t_{LOW}	Clock Pulse Width Low	0.16	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.06	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.01	-	0.14	μs
t_I	Noise Suppression Time	-	-	0.01	μs
t_{BUF}	Time the bus must be free before a new transmission can start	0.3	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.16	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.16	-	-	μs
$t_{HD.DAT}$	Data in Hold Time	0	-	-	μs
$t_{SU.DAT}$	Data in Setup Time	0.01	-	-	μs
t_R	Inputs Rise Time[1]	0.01	-	0.08	μs
t_F	Inputs Fall Time[1]	0.01	-	0.08	μs
$t_{SU.STO}$	Stop Setup Time	0.16	-	-	μs
t_{DH}	Data Out Hold Time	0.01	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	ms

Notes: [3] AC measurement conditions:

- t_{AA} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 VCC or 0.7 VCC, assuming that Rbus × Cbus time constant is within 20 ns
- RL (connect to VCC): 1.3 kΩ
- CL = 15 pF
- Input pulse voltage: 0.2 VCC to 0.8 VCC
- Input rise and fall time: < 50 ns
- Input and output timing reference voltage: 0.3 VCC and 0.7 VCC

Table 3-6 Reliability Characteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

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Figure 3-1 Bus Timing

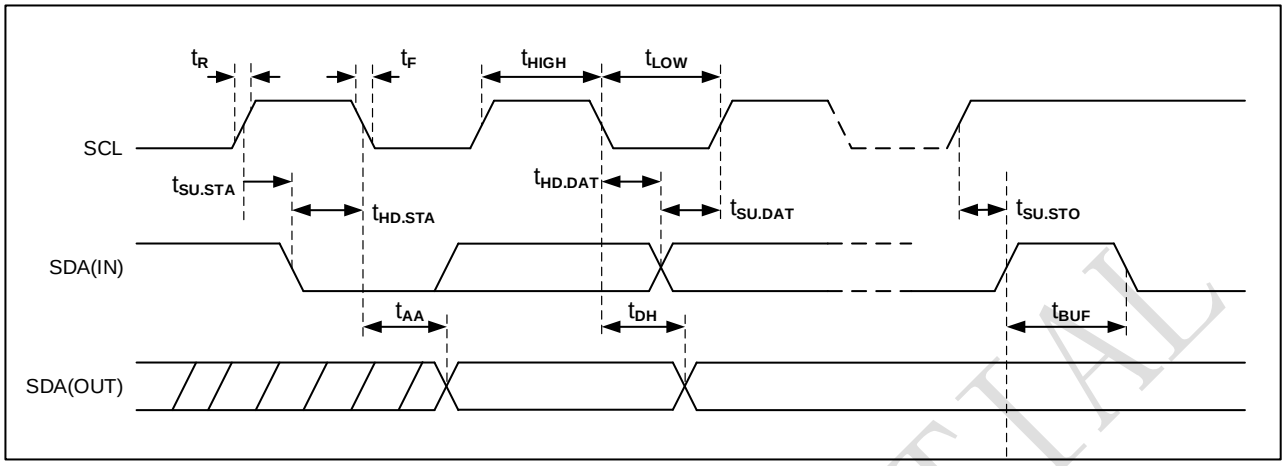
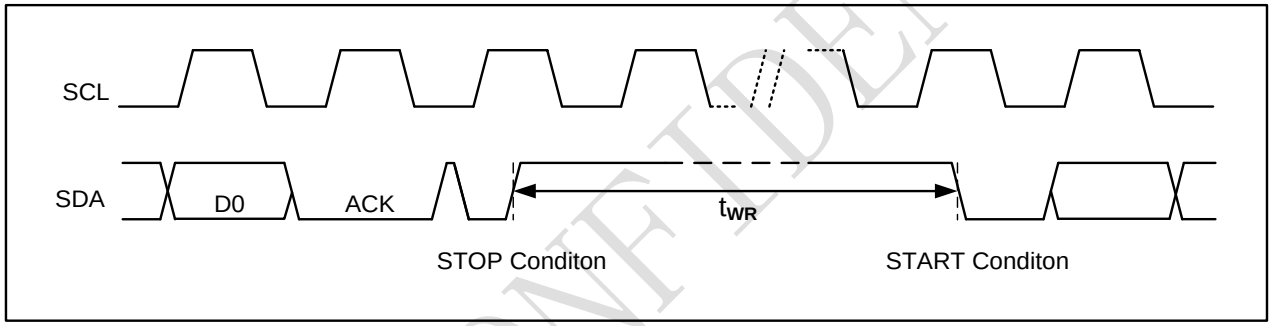


Figure 3-2 Write Cycle Timing



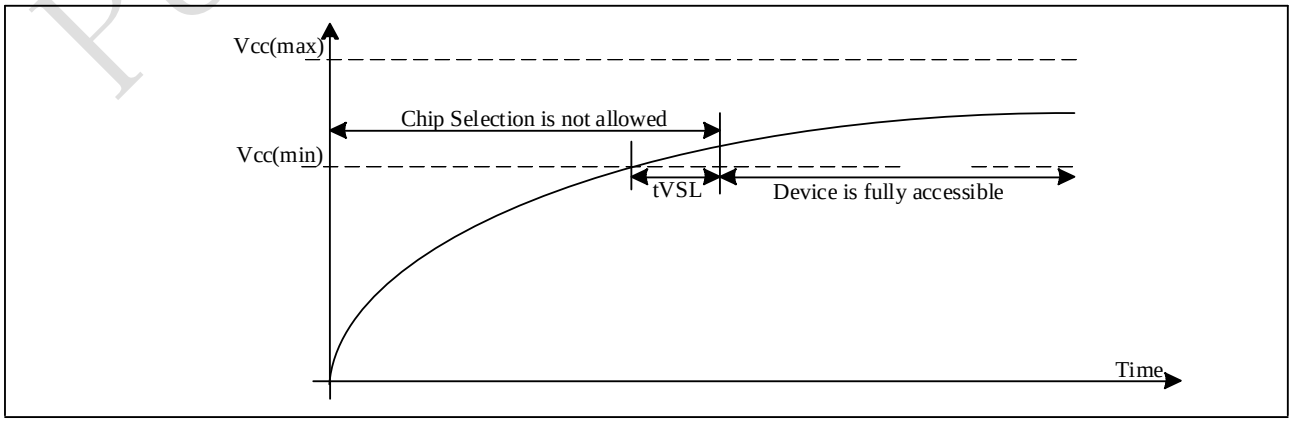
Note: [1] The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal write cycle.

Device Power-Up

The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status. tVSL is the time required to initialize the EEPROM. No instructions are accepted during this time.

Figure 3-3 Power up Timing



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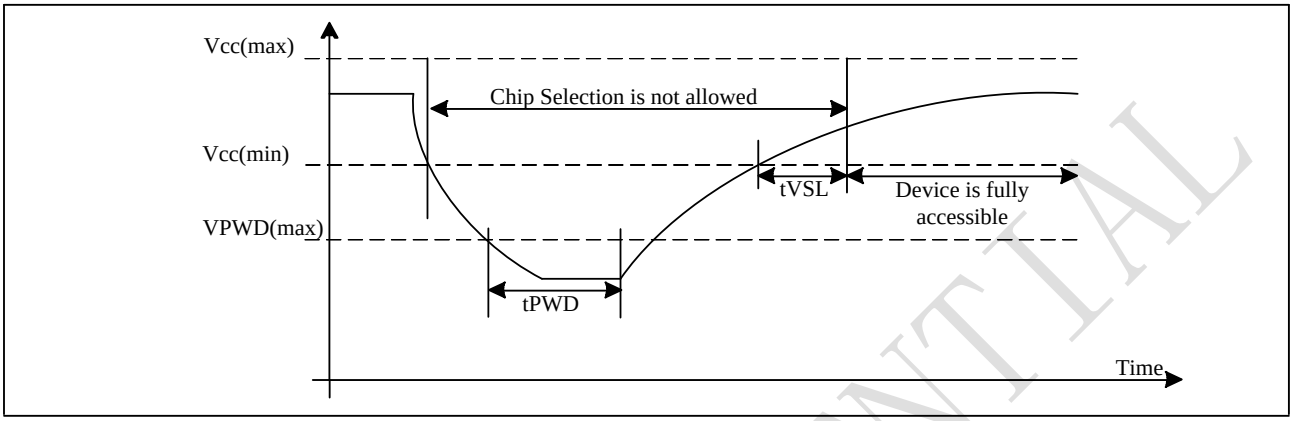
Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of EEPROM device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 3-4 Power down-up Timing



Symbol	Parameter	min	max	unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	100		us
tVR	VCC Rise Time	1	500000	us/V

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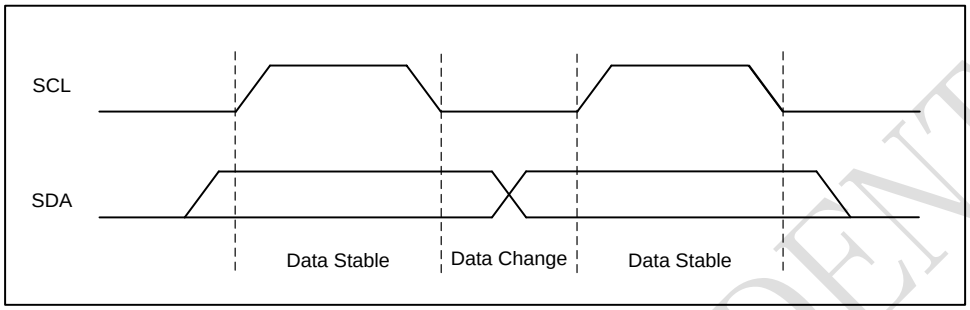
4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined in Figure 4-2.

Figure 4-1 Data Validity



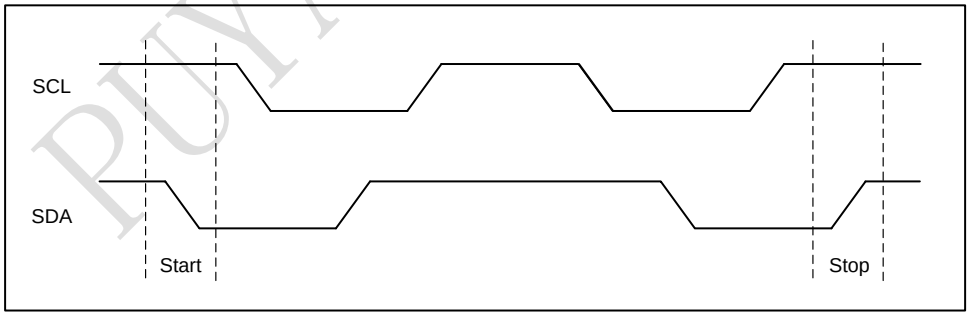
4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the P24C512X in a standby mode (see Figure 4-2).

Figure 4-2 Start and Stop Definition



4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the P24C512X in 8-bit words. The P24C512X sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

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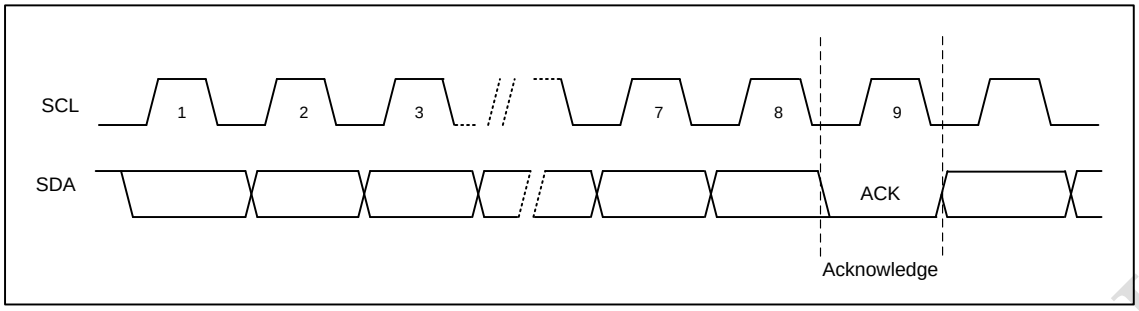
Figure 4-3 Output Acknowledge



4.5 Power Up Sequence

During a power-up sequence, the V_{CC} supplied to P24C512X should monotonically rise from Vss to the minimum V_{CC} level with a slew rate no greater than 1us/V.

To prevent inadvertent write operations or other spurious events from happening during a power-up sequence, theP24C512X includes a power-on-reset circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold and waiting 100μs that brings the device out of reset and into standby mode.

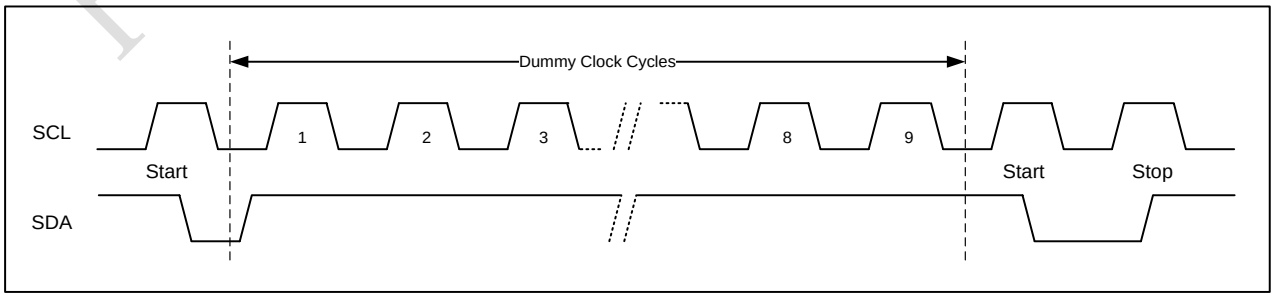
4.6 Standby Mode

The P24C512X features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

4.7 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



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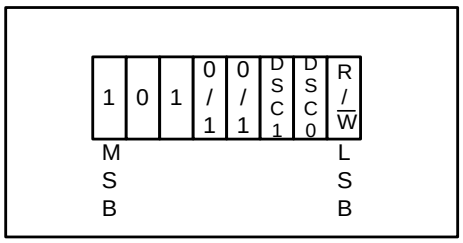
4.8 Device Addressing

The P24C512X requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4-5). The device address word consists of a mandatory 1010B and 1011B sequence for the first four most-significant bits respectively for normal memory area access, ID page, Lock bit, SWP register or DSC register access.

Figure 4-5 Device Address



The two DSC1, and DSC0 device address bits allow as many as four devices on the same I²C-compatible bus. These bits must compare to the corresponding internal Device Select Code (DSC) setting.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a match of the device address, the Chip will output a zero as an ACK. If not match, a NACK of high level shall be output and the device will return to the standby state.

Following the device address, two-byte word address is adopted to access the normal memory area, ID page, Lock bit, SWP register or DSC register.

Table 4-1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C512X	Normal Area	1	0	1	0	0	DSC1	DSC0	R/W
	ID Page	1	0	1	1	1	DSC1	DSC0	R/W
	Lock Bit	1	0	1	1	1	DSC1	DSC0	R/W
	SWP REG	1	0	1	0	1	DSC1	DSC0	R/W
	DSC REG	1	0	1	0	1	DSC1	DSC0	R/W

Note:

1. The Device Select Code DSC1/DSC0 is software programmable by DSC register write.

Table 4-2 Word Address0

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C512X	Normal Area	A15	A14	A13	A12	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	X	1	X	X
	SWP REG	1	0	1	X	X	X	X	X
	DSC REG	1	1	0	X	X	X	X	X

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Table 4-3 Word Address1

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C512X	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	X	X	A5	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	SWP REG	X	X	X	X	X	X	X	X
	DSC REG	X	X	X	X	X	X	X	X

4.9 Data Security

P24C512X has a software data protection scheme that allows the user to write protect the memory. Please refer to the section 5.1.6 for detail.

4.10 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes [1]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group [1]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value.

Note: [1]A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer

4.11 High Speed Mode (HS-mode)

The P24C512X supports 3.4MHz high speed mode. A master code (00001XXXb) must be issued to place the device into high speed mode. Communication between master and slave will then be enabled for speeds up to 3.4-MHz. A STOP condition will exit HS-mode. Single- and multiple-byte reads and writes are supported.

Figure 4-6 High Speed Communication

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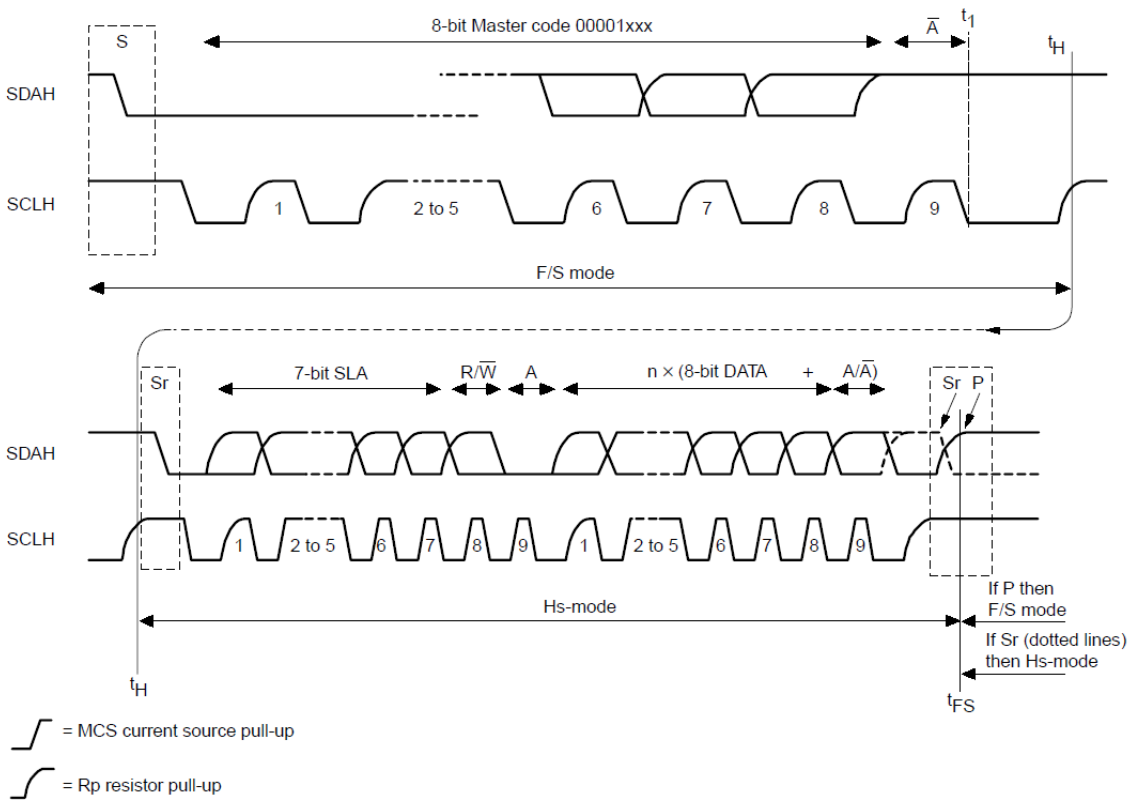

Sr: Repeated Start Flag

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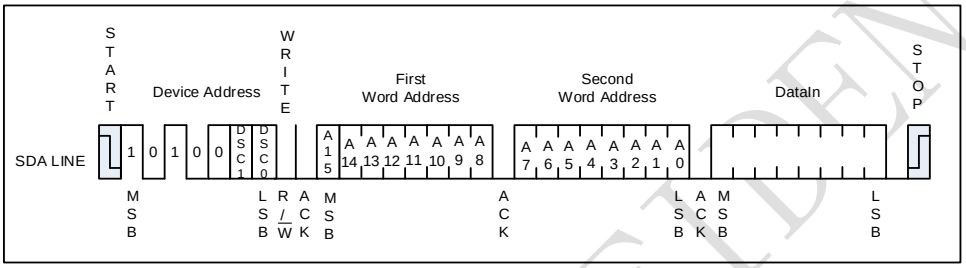
5. Instructions

5.1 Write Operations

5.1.1 Byte Write

A write operation requires two 8-bit data word address (A15~A0) following the device address word and acknowledgment. Upon receipt of this address, the P24C512X will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the P24C512X will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the P24C512X enters an internally timed write cycle, all inputs are disabled during this write cycle and the P24C512X will not respond until the write is complete (see Figure 5-1).

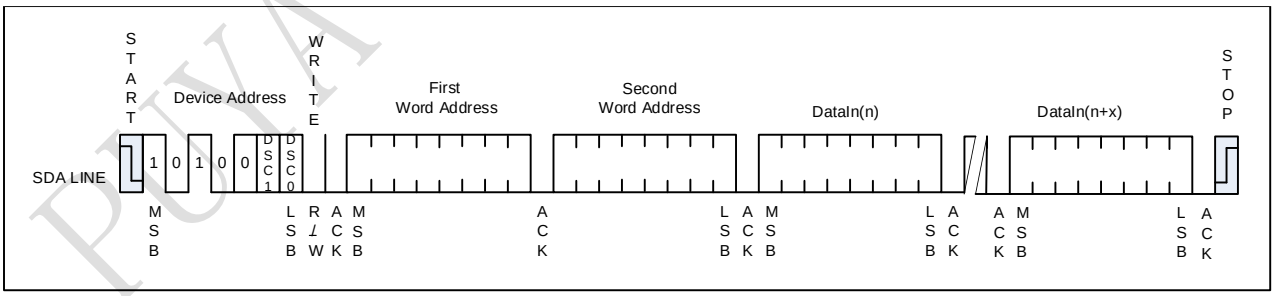
Figure 5-1 Byte Write



5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the P24C512X acknowledges receipt of the first data word, the master can transmit more data words. The P24C512X will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 5-2 Page Write



The lower seven bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the P24C512X, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

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5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the P24C512X inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the P24C512X respond with a “0”, allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (128 bytes) is an additional page which can be written and later permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write, except for the following differences:

- Device type identifier = 1011b
- MSB address A11 and A10 must be “0” while other bits in A15~A7 are don’t care.
- LSB address bits A6~A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock Bit Write Instruction) permanently locks the Identification page in Read-only mode. The Lock ID Page instruction is similar to Byte Write with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

5.1.6 Soft Write Protection& Device Select Code Settings

By writing specific values in the SWP register (Table 5-1) located at address 101x_xxxx_xxxx_xxxxB, the memory array can be write-protected. Bits b7, b6, b5, b0 of the data byte for registers are not significant (Don't Care).

By writing specific values in the DSC register (Table 5-2) located at address 110x_xxxx_xxxx_xxxxB, the Device Select Code (DSC) can be changed. Bits b7, b6, b5, b4, b0 of the data byte for registers are not significant (Don't Care).

Both registers are accessed by command device address of {1010, 1, DSC [1:0], r/w} and both registers are non-volatile.

Writing more than one byte will discard the write cycle, that is, the two registers’ content will not be changed under this condition.

Table5-1 SWP Register @101x_xxxx_xxxx_xxxxB Address

Bit	7	6	5	4	3	2	1	0	Default
Bit Definition	-	-	-	CMDCFG	SWPEN	SWPB1	SWB0	-	/
R/W	RO	RO	RO	RW	RW	RW	RW	RO	/
Default	0	0	0	0	0	0	0	0	00H

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Table 5-2 DSC Register @110x_xxxx_xxxx_xxxxB Address

Bit	7	6	5	4	3	2	1	0	Default
Bit Definition	-	-	-	-	DSC2	DSC1	DSC0	/	/
R/W	RO	RO	RO	RO	RW	RW	RW	RO	/
Default	0	0	0	0	0	0	0	0	00H

Table 5-3 Bit Definition for SWP Register

Bit	Definition	Description	Defaults	Note
7~5	/	Reserved for future use	000B	
4	Command device ID	Set command device ID 0: A0/B0, A1/B1 1: C0/D0, C1/D1 Refer to the Table5-5	0B	
3	Write protect activation	Enables or disables the Write protection 0: the whole memory can be written (no Write protection) 1: the concerned block is write-protected	0B	
2~1	Size of write protected block	Define the size of the memory block to be protected against write instructions 00: the upper quarter of memory is write-protected 01: the upper half memory is write-protected 10: the upper 3/4 of memory are write-protected 11: the whole memory is write-protected	00B	
0	/	Reserved for future use	0B	

Table 5-4 Bit Definition for DSC Register

Bit	Definition	Description	Defaults	Note
7~4	/	Reserved for future use	0000B	
3~1	DSC[2:0]	The Device ID of the EEPROM is constructed as {1011/1010, 0/1, DSC [1:0], R/W}. DSC [1:0] is defined as Device Select Code.	000B	
0	/	Reserved for future use	0B	

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Table 5-5 Command Device ID

CMDCFG	Device ID	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	A0	1	0	1	0	0	DSC1	DSC0	W
	A1	1	0	1	0	0	DSC1	DSC0	R
	B8	1	0	1	1	1	DSC1	DSC0	W
	B9	1	0	1	1	1	DSC1	DSC0	R
1	C0	1	1	0	0	0	DSC1	DSC0	W
	C1	1	1	0	0	0	DSC1	DSC0	R
	D8	1	1	0	1	1	DSC1	DSC0	W
	D9	1	1	0	1	1	DSC1	DSC0	R

5.2 Read Operations

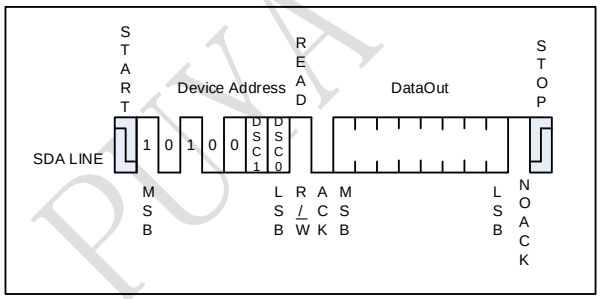
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the P24C512X, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 5-3).

Figure 5-3 Current Address Read



5.2.2 Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the P24C512X, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The P24C512X acknowledges the device address and serially clocks out the data word. The microcontroller responds with a “1” and generates stop condition (see Figure 5-4) followed.

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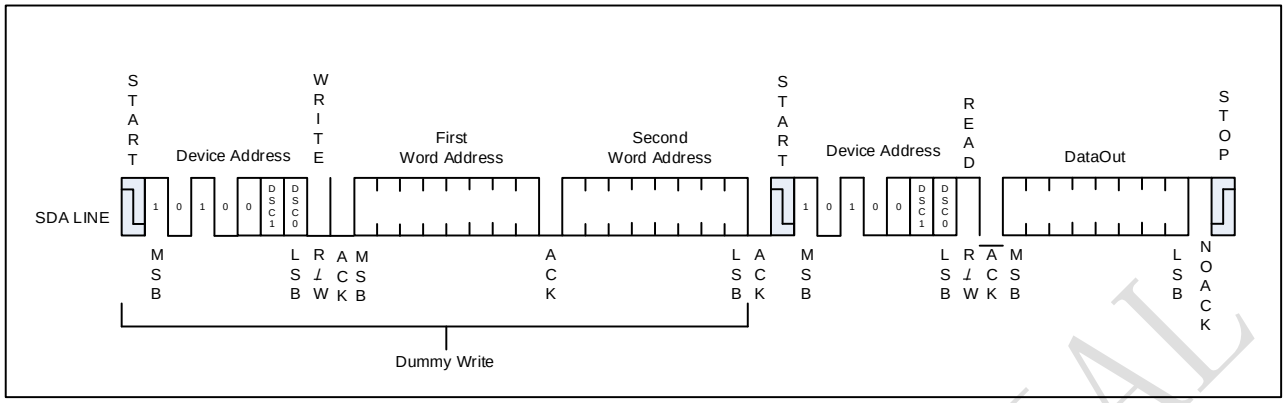
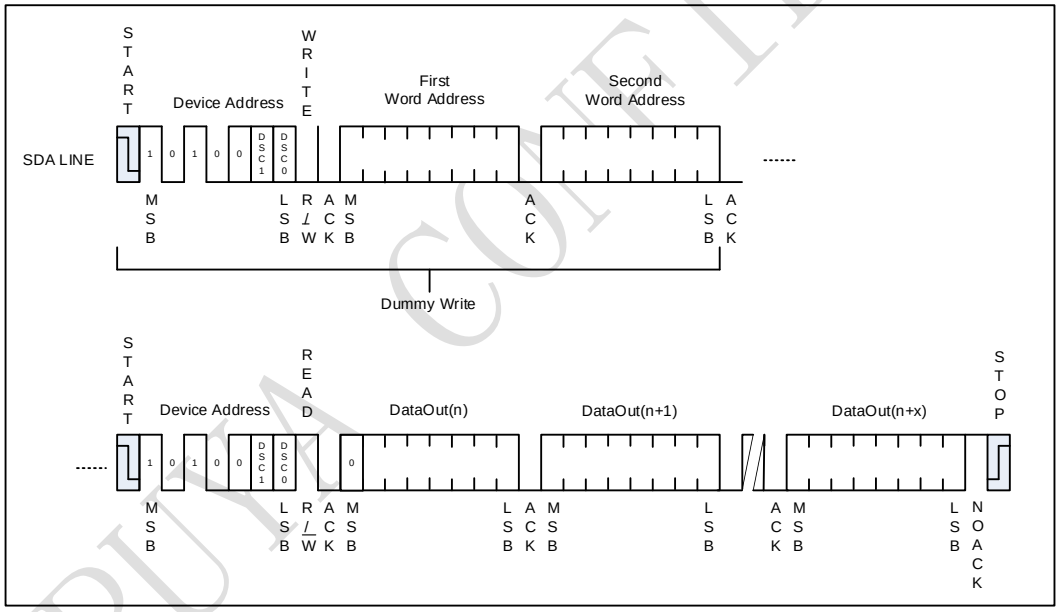
Figure 5-4 Random Read



5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the P24C512X receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller responds with a "1" and generates a stop condition (see Figure 5-5) followed.

Figure 5-5 Sequential Read



5.2.4 Read Identification Page

The Identification Page (128 bytes) is an additional page which can be written and later permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command with device type identifier defined as 1011b. The MSB address bits A15~A7 are don't care, the LSB address bits A6~A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. When reading the Identification Page from location 10d, the number of bytes should be less than or equal to 118, as the ID page boundary is 128 bytes).

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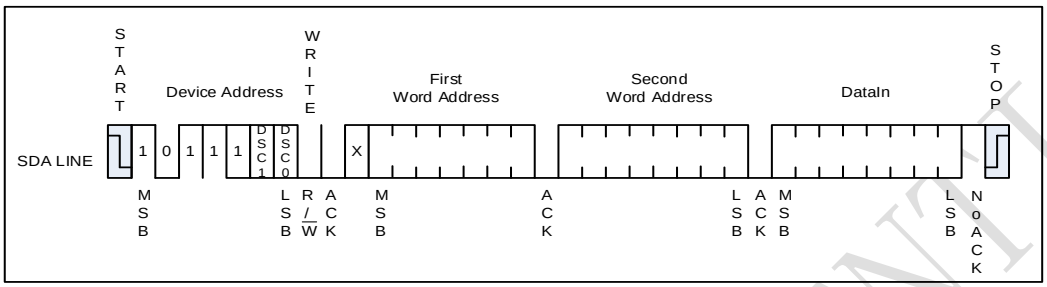
5.2.5 Read Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NO-ACK bit if the Identification page is locked.

Figure 5-6 Lock Status Read (When Identification page locked, return NO-ACK after one data byte)



5.2.6 Read SWP and DSC Registers

Reading the SWP register is similar to the sequential read sequence with device address {1010, 1, DSC [1:0], r/w} and address 101x_xxxx_xxxx_xxxxB;

Reading the DSC register is similar to the sequential read sequence with device address {1010, 1, DSC [1:0], r/w } and address 110x_xxxx_xxxx_xxxxB;

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6. Ordering Code Detail

Example: P 2 4 C 512 X – C4 H – M I R

Company Designator

P = Puya Semiconductor

Product Series Name

24C = I2C-compatible Interface EEPROM

Device Density

512 =512K bits

Device Reversion

X = Version X

Package Option

C4: WLCSP4 (Ball Pitch 400umX400um)

D4: WLCSP4 (Ball Pitch 400umX500um)

Plating Technology

H: RoHS Compliant, Halogen-free

Operation Voltage

M: 1.65~3.6V

Device Grade

I: -40~85C

Shipping Carrier Option

R: TAPE& REEL

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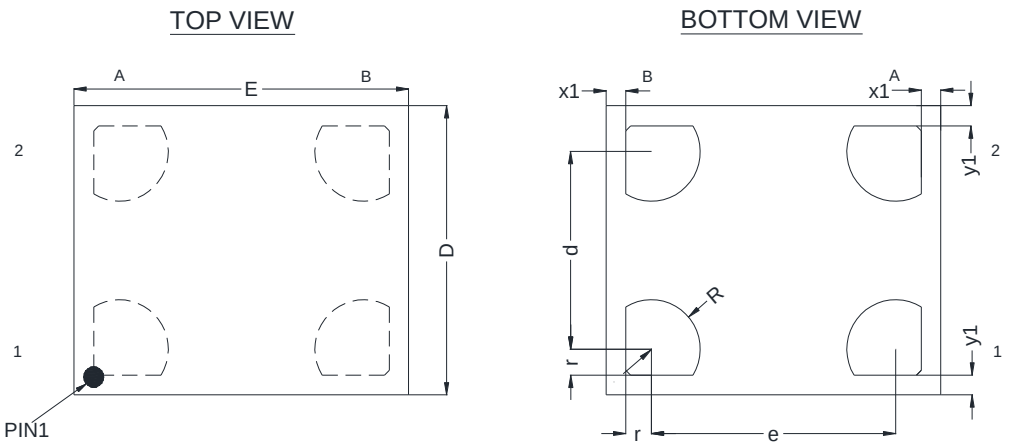
7. Package information

7.1 WLCSP4 (Ball Pitch 400um*500um)



PIN ASSIGNMENT MATRIX

	A	B
2	SCL	Vss
1	Vcc	SDA

NOTE: 1.Dimensions are NOT to scale.
2.Solder ball composition is SnAg.
3.Product offered with Back Side Coating(BSC)

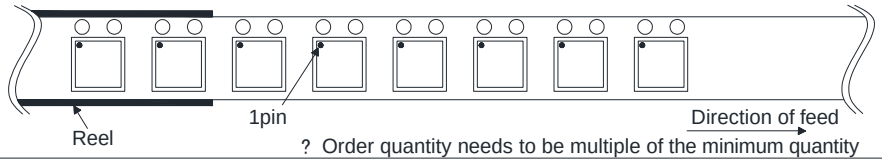
COMMON DIMENSIONS
(Unit of Measure =mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.255	0.280	0.305	
A1	0.050	0.055	0.060	
A2	0.180	0.200	0.220	
A3		0.025BSC		
D	0.555	0.585	0.615	
d	-	0.400	-	
y1		0.04REF		
E	0.655	0.685	0.715	
e	-	0.500	-	
x1		0.04REF		
R	-	0.1000	-	
r	-	0.0525	-	

	TITLE	DRAWING NO.	REV
PUYA	4-ball,2x2 Array,0.4x0.5mm pitch Wafer Level Chip ScalePackage with BSC	DS-4	B

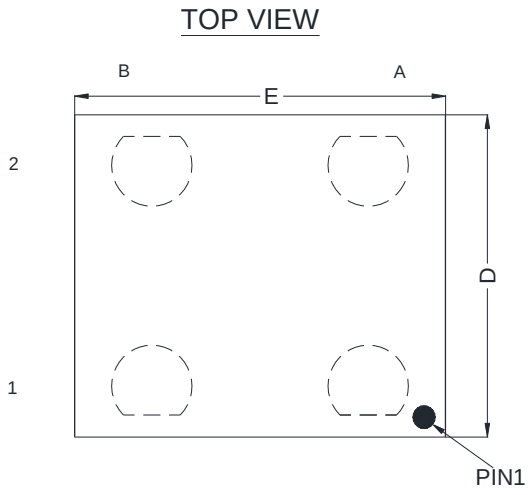
<Tape and Reel information>

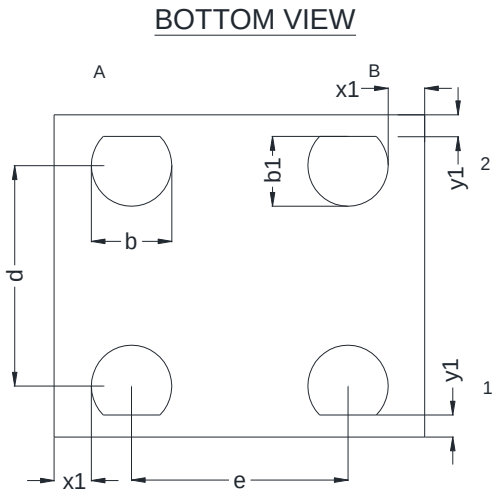
Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

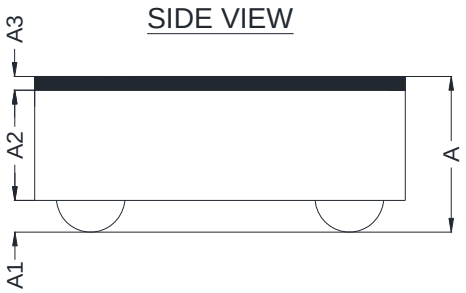


? Order quantity needs to be multiple of the minimum quantity

7.2 WLCSP4 (Ball Pitch 400um*400um)







COMMON DIMENSIONS
(Unit of Measure =mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.255	0.280	0.305	
A1	0.050	0.055	0.060	
A2	0.180	0.200	0.220	
A3		0.025BSC		
D	0.555	0.585	0.615	
d	-	0.400	-	
y1		0.04REF		
E	0.655	0.685	0.715	
e	-	0.400	-	
x1		0.052REF		
b	-	0.180	-	
b1	-	0.142	-	

PIN ASSIGNMENT MATRIX

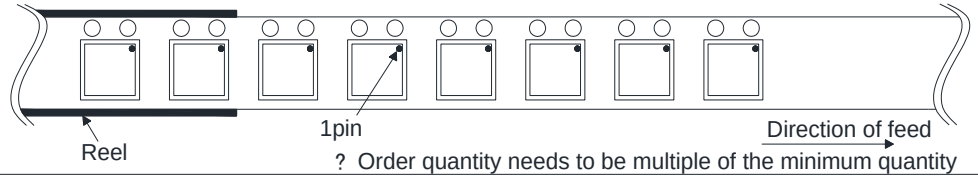
	B	A
2	SDA	SCL
1	Vss	Vcc

NOTE: 1.Dimensions are NOT to scale.
2.Solder ball composition is SnAg.
3.Product offered with Back Side Coating(BSC)

	TITLE	DRAWING NO.	REV
PUYA	4-ball,2x2 Array,0.4mm pitch Wafer Level Chip ScalePackage with BSC	CS-4	B

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



? Order quantity needs to be multiple of the minimum quantity

8. Revision History

Version	Content	Date
Rev 1.0	Initial Release	2020-12-20
Rev 1.1	Update Device Addressing and some descriptions Add 7. Valid Part Numbers and Top Marking	2021-07-20
Rev 1.2	Add package of WLCSP4 (Ball Pitch 400umX500um)	2023-01-03
Rev 1.3	Update Table 3-1	2023-02-16

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